# ECEN 215 – PRIN OF ELECTRICAL ENGR

# Fall 2018

## Lab 8: Introduction to Logic Gates



**Submitted by:**

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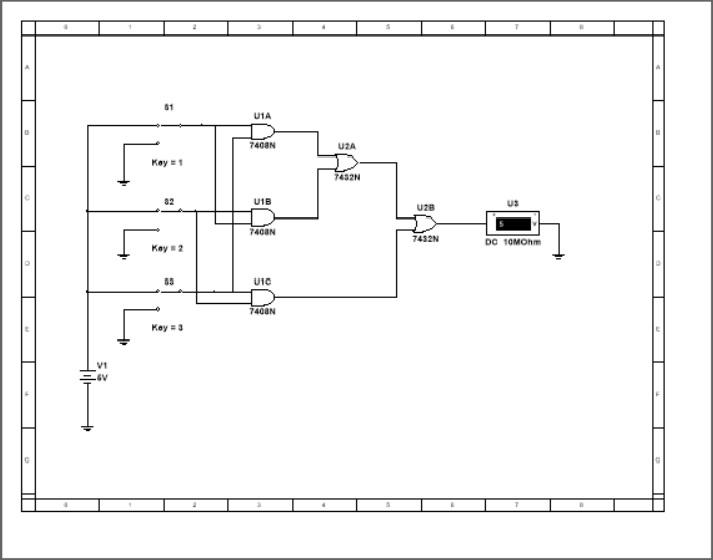
**Date Performed: Feb 4th , 2019**

1. **Objective**

The objective of the lab was to first test the two logic components (AND and OR gates), and then use them to construct a circuit with three switches that outputs a high voltage (approximately 5V) when two or more of the switches are closed.

1. **Procedure**
2. Connect the AND gate (7408) and the OR gate (7432) to the voltage source and grounds. Then test each input by measuring the output voltage and comparing to the truth tables (tables 1 and 2 in Results) for the corresponding gate. Use the measured output voltages to fill out truth tables for both devices.
3. Construct the circuit according to the diagram in Figure 1 (see Results).
4. Measure and record the actual output voltage of the source. For every permutation of open/closed switches, record the resulting output voltage in table 3 (see Results). Closed switch refers to the recorded output voltage of the source (approximately 5V, binary value of 1) source and open switch refers to the ground (binary value of 0). The resulting voltages are of the categories high (Vout is approximately 5V, binary value of 1) and low (Vout is approximately 0V, binary value of 0).
5. Compare results to theoretical truth table from prelab (Table 4 in Results)
6. **Difficulties**
7. When creating actual switch circuits, the voltage source would shut off due to overcurrent issues. We were only successful when attaching the inputs to the source and ground.
8. Keeping the wires inside the Analog Discovery.
9. **Results**

**Figures**



(Figure 1—Circuit Diagram)

**Individual Gate Tables**

**Table 1 (AND gate):**

|  |  |  |
| --- | --- | --- |
| A | B | Vout (V) |
| 0 | 0 | 0.183 |
| 0 | 1 | 0.235 |
| 1 | 0 | 0.193 |
| 1 | 1 | 4.507 |

**Table 2 (OR gate):**

|  |  |  |
| --- | --- | --- |
| A | B | Vout (V) |
| 0 | 0 | 0.205 |
| 0 | 1 | 4.231 |
| 1 | 0 | 4.377 |
| 1 | 1 | 4.439 |

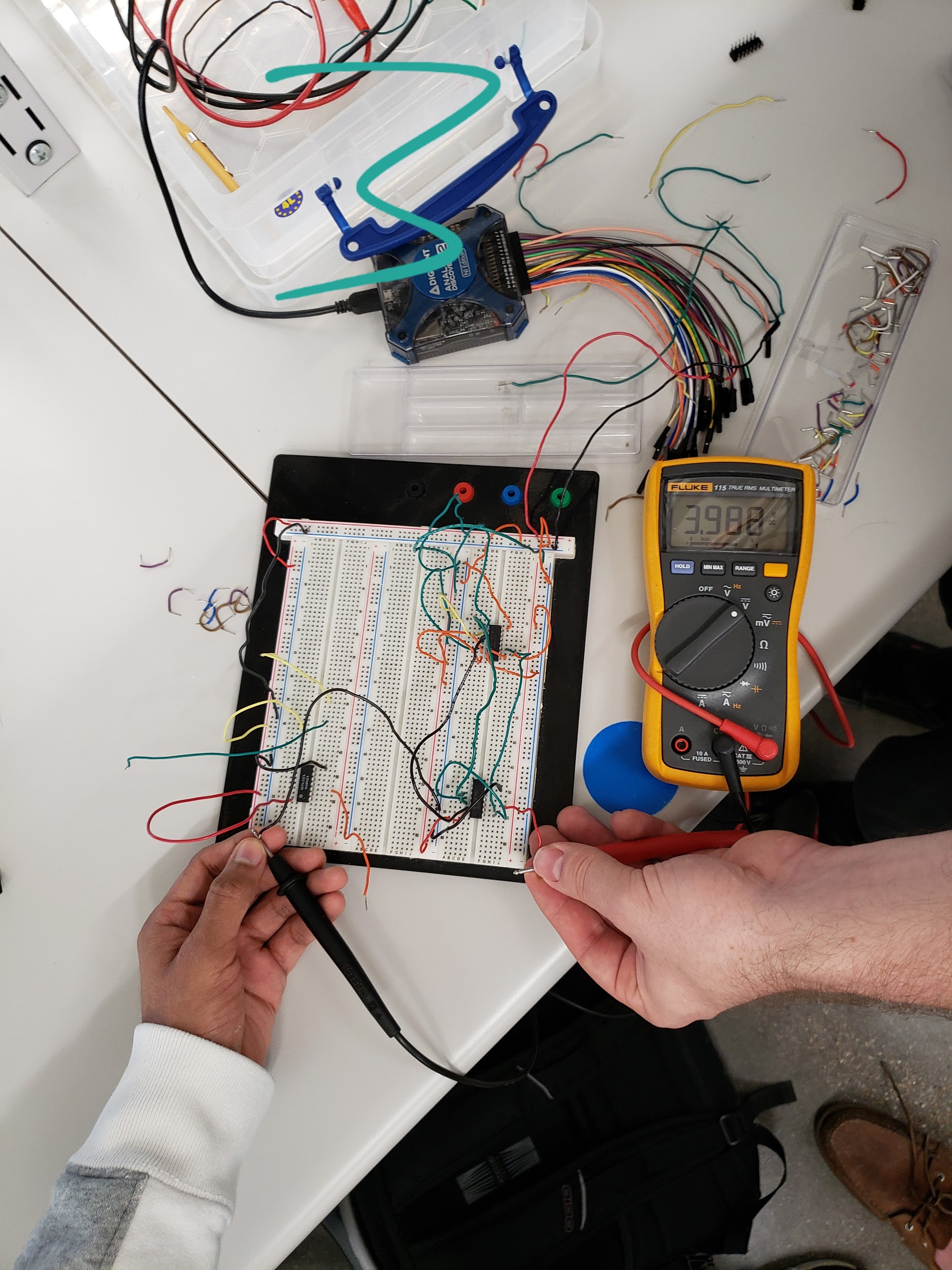
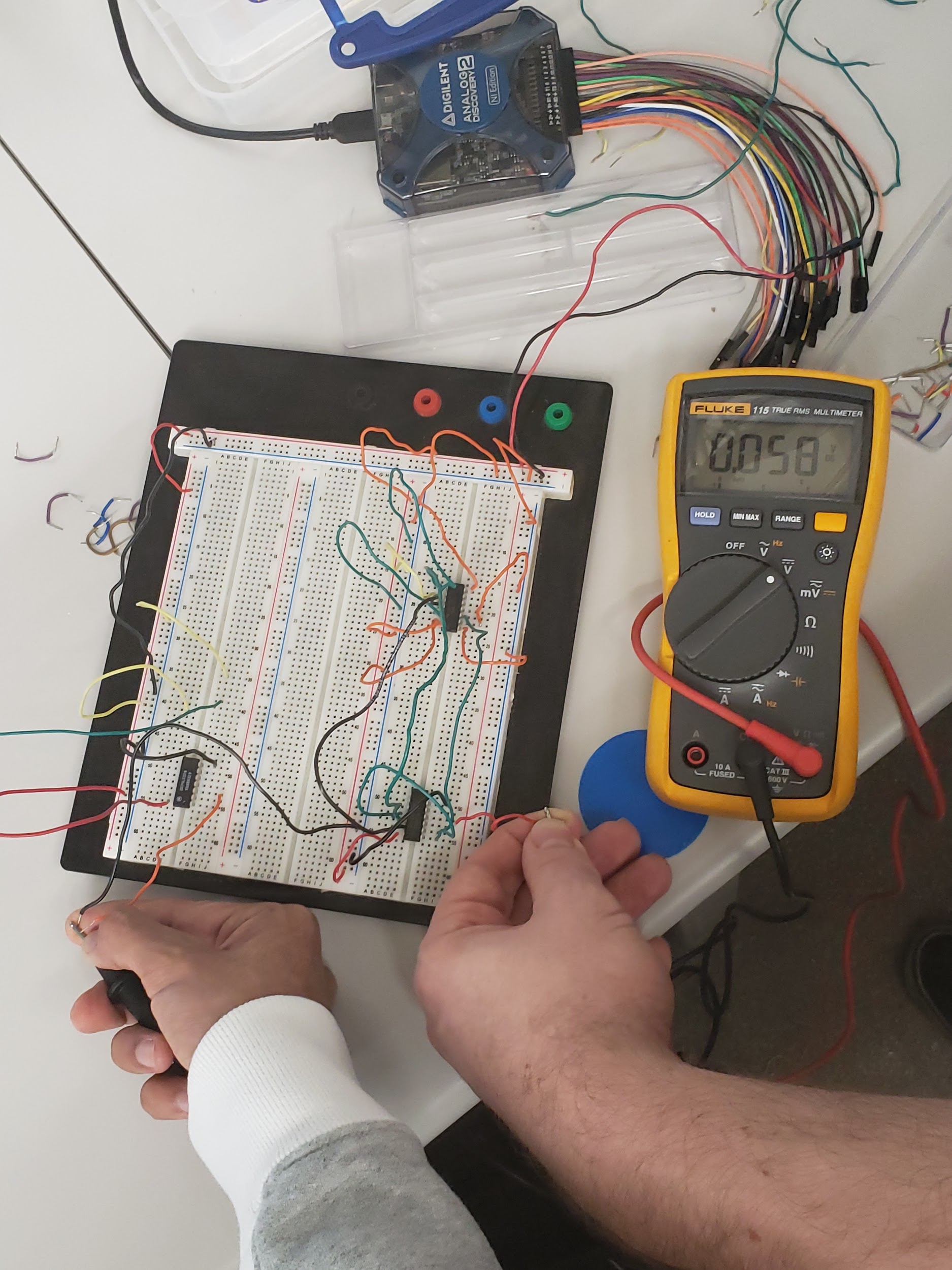
**Full Circuit Tables**

**Table 3 (Full Circuit Actual):**

|  |  |  |  |
| --- | --- | --- | --- |
| A (V) | B (V) | C (V) | Vout (V) |
| 0 | 0 | 0 | 0.172 |
| 0 | 0 | 4.938 | 0.190 |
| 0 | 4.938 | 0 | 0.184 |
| 0 | 4.938 | 4.938 | 4.518 |
| 4.938 | 0 | 0 | 0.171 |
| 4.938 | 0 | 4.938 | 4.234 |
| 4.938 | 4.938 | 0 | 4.511 |
| 4.938 | 4.938 | 4.938 | 4.303 |

**Table 4 (Full Circuit Theoretical):**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| A (V) | B (V) | C (V) | Vout (V) | |Vtheoretical - Vactual| |
| 0 | 0 | 0 | 0 | 0.172 |
| 0 | 0 | 5 | 0 | 0.190 |
| 0 | 5 | 0 | 0 | 0.184 |
| 0 | 5 | 5 | 5 | 0.482 |
| 5 | 0 | 0 | 0 | 0.171 |
| 5 | 0 | 5 | 5 | 0.766 |
| 5 | 5 | 0 | 5 | 0.489 |
| 5 | 5 | 5 | 5 | 0.697 |

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1. **Conclusion**

This experiment shows that gates can be used to control a single output voltage with complex relationships between switches at the inputs. Using the materials provided, we also found that constructing our own switching circuits had unexpected results. We are not certain as to the reason for this, but did find that if the inputs to the gates are not properly grounded they do not function as intended. It is therefore our hypothesis that this occurs because the ground for the gate component is not attached to the inputs; therefore if the switches are not properly grounded when opened, the gates will not function properly.